Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the present application.

Claim Listing

1-19. (Cancelled)

20. (Currently Amended) A circuit for checking the integrity of one or more input vectors to a digital hardware block, comprising:

a memory array containing a weight matrix having elements which are based on a set of known bad input vectors for the digital hardware block; ~~and~~

means for selectively classifying future input vectors to the digital hardware block as either good or not good, using the weight matrix, wherein the classifying means classifies a given input vector as good or not good in less than 60 ns;

an SRAM array;

a content-addressable memory for storing the known bad input vectors; and

address management means for using said SRAM to update both the content-addressable memory and the weight matrix.

21. (Original) The circuit of Claim 20 further comprising means for creating the weight matrix using a feedforward linear associative memory neural network.

22. (Original) The circuit of Claim 20 wherein said classifying means classifies as not good both future input vectors which are definitely faulty and future inputs vectors which are potentially faulty.

23. (Original) The circuit of Claim 20 wherein the weight matrix W is created using a discrete Hopfield network algorithm according to the equation

$$w_{ij} = \sum_{m=1}^{M} (2a_i^{(m)} - 1)\,(2b_j^{(m)} - 1)$$

where $a^{(m)}$ is the set of known bad vectors, $a_i = b_j$, M is the number of bad input vectors in the set of known bad input vectors, i is a row locator representing a particular bad vector, and j is a column locator representing a bit location.

24. (Original) The circuit of Claim 23 wherein said classifying means includes means for calculating an output vector $a^{(m)}$ by multiplying the weight matrix W by the new input vector $b^{(m)}$, that is, $a^{(m)} = Wb^{(m)}$.

25. (Original) The circuit of Claim 24 wherein said classifying means further includes means for adjusting elements of the output vector $a^{(m)}$ by its respective thresholds θ_i according to the equation

$$\theta i = - \tfrac{1}{2} \sum_{j=1}^{K} w_{ij}$$

where K is the total number of bits in a vector.

26. (Original) The circuit of Claim 25 wherein said classifying means includes a plurality of non-linear units which respectively processes the adjusted elements such that, when a given adjusted element is positive, an output of the corresponding non-linear unit is 1 and, when a given adjusted element is not positive, the output of the corresponding non-linear unit is 0.

27. (Cancelled)

28. (Currently Amended) The circuit of Claim 20 further comprising ~~mean~~ means for blocking an output of the digital hardware block corresponding to a new input vector, and accepting an output of a software work-around corresponding to the new input vector, in response to said classifying means classifying the new input vector as not good.

29. (Original) The circuit of Claim 20 further comprising means for updating the weight matrix online using one or more additional bad input vectors.

30-32. (Cancelled)

33. (Original) A programmable logic unit comprising:

a plurality of interconnected hardware blocks, at least one of said hardware blocks being a faulty hardware block;

a feedforward linear associative memory (LAM) neural network checking circuit which classifies input vectors to said faulty hardware block as either good or not good;

a software work-around input; and

a selection circuit connected to said feedforward LAM neural network checking circuit, for (i) blocking an output vector of the faulty hardware block corresponding to a new input vector, (ii) enabling a software work-around for the new input vector, and (iii) accepting an output vector from said software work-around input corresponding to the new input vector, as an output vector of the programmable logic circuit.

34. (Original) The programmable logic unit of Claim 33 wherein said selection circuit includes:

a software work-around enable signal output of said feedforward LAM neural network checking circuit; and

a multiplexer having two inputs respectively receiving the output vector from said faulty hardware block and the output vector from said software work-around, and a select line which is connected to said software work-around enable signal output of said feedforward LAM neural network checking circuit.

35. (Original) The programmable logic unit of Claim 33 wherein said feedforward LAM neural network checking circuit has a weight matrix whose elements are based on a set of known bad input vectors for said faulty hardware block.

36. (Original) The programmable logic unit of Claim 35 wherein said

feedforward LAM neural network checking circuit updates the weight matrix online using one or more additional bad input vectors.

37. (Original) The programmable logic unit of Claim 36 wherein said feedforward LAM neural network checking circuit includes:

an SRAM array;

a content-addressable memory for storing the known bad input vectors; and

address management means for using said SRAM to update both said content-addressable memory and said weight matrix.

38. (Original) The programmable logic unit of Claim 35 wherein the weight matrix W in said feedforward LAM neural network checking circuit is calculated according to the equation

$$w_{ij} = \sum_{m=1}^{M} (2a_i^{(m)} - 1)(2b_j^{(m)} - 1)$$

where $a^{(m)}$ is the set of known bad vectors, $a_i = b_j$, M is the number of bad input vectors in the set of known bad input vectors, i is a row locator representing a particular bad vector, and j is a column locator representing a bit location.

39. (Original) The programmable logic unit of Claim 38 wherein said feedforward LAM neural network checking circuit includes:

means for calculating an output vector $a^{(m)}$ by multiplying the weight matrix W by the new input vector $b^{(m)}$, that is, $a^{(m)} = Wb^{(m)}$;

means for adjusting elements of the output vector $a^{(m)}$ by its respective thresholds θ_i according to the equation

$$\theta i = - \tfrac{1}{2} \sum_{j=1}^{K} w_{ij}$$

where K is the total number of bits in a vector; and

a plurality of non-linear units which process respective elements of the weight matrix to provide an output of 1 when a given adjusted element is positive, and provide an output of 0 when a given adjusted element is not positive.

40. (Original) The programmable logic unit of Claim 39 wherein said feedforward LAM neural network checking circuit matches a vector constructed of the outputs of said non-linear units with an entry in a content-addressable memory storing the set of known bad vectors.

41. (Original) The programmable logic unit of Claim 33 wherein said feedforward LAM neural network checking circuit classifies input vectors to said faulty hardware block as either good or not good prior to said faulty hardware generating its output vector corresponding to the new input vector.

42. (Original) The programmable logic unit of Claim 33 wherein said feedforward LAM neural network checking circuit is physically located in a re-configurable hardware redundancy block.